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EXAMINER	
KHOSRAVIANI, ARMAN	
ART UNIT	PAPER NUMBER
2818	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,340	IIHOLA ET AL.	
	Examiner	Art Unit	
	Arman Khosraviani	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-7 and 10-19* is/are pending in the application.

4a) Of the above claim(s) *5 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear, when components are embedded in at least two sheets, which of these two sheets are subsequently attached on top of each other. In order to advance prosecution, Examiner will interpret claim 13 to mean "components are embedded in at least two sheets, [wherein the second sheet is] subsequently attached on top of [the first sheet.]"

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear, when components are embedded in at least two sheets, which of these two sheets are subsequently attached on top of each other. Elements in the first six process steps of claim 3, taken directly from claim 1, conflict with elements in the remaining five process steps, making claim 3 indefinite. It is necessary for Applicant to distinguish between the two recesses and the two conductive layers, because a first component corresponds to a first recess. For example, changing the language in the second process step from "making at least one recess in the sheet…as far as the conductive layer…which covers the recess" to – making at least

one recess…the first conductive layer on the first surface…which forms and covers a first recess –.

Claim Objections

3. Claim 16, line 10 is objected to because of the following informalities: "contact surface of the component facing the first surface" should be replaced with -- contact surface of the first component facing the first surface --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 10-11, 15 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shindo et al. (US 5,048,179).

Regarding claim 1, Shindo teaches (e.g. figures 23-24, see also column 6, line 3 – column 7, line 10) a method for manufacturing an electronic module, comprising: taking a sheet 42, which has a first and a second surface, and which sheet includes an insulating-material layer (plastic) between the first and the second surface, as well as a conductive layer 58 on at least the first surface making at least one recess 44 in the sheet that extends through the second surface and the insulating-material layer as far as the conductive layer 58 on the first surface, which covers the recess from the

direction of the first surface (58 of figure 24), taking a component 50 having a contact surface with contact areas or contact protrusions, placing the component in the recess with its contact surface facing the first surface, attaching the component to the conductive layer, which covers the recess from the direction of the first surface (col. 6, ll. 31-46), by gluing with the aid of an electrically insulating adhesive 46, and forming a conductive pattern from the conductive layer covering the recess and forming an electrical contact 58 between the component and the conductive pattern (col. 6, ll. 4-14) by making feed-throughs 54, 56 (contact holes), which connect at least some of the contact areas or contact protrusions of the component electrically to, the conductive pattern.

Regarding claim 10, Shindo teaches (e.g. figures 23-24, see also col. 6, ll. 38-46) the method above, wherein at least one component is attached, and electrical contact with the conductive layer is formed by bonding the contact areas (contact holes and pads) metallurgically (58 is copper) to the conductive layer (deposition of copper), either directly, or through intermediary contact protrusions.

Regarding claim 11, Shindo teaches (e.g. figures 23-24, see also column 6, line 3 – column 7, line 10) the method above, wherein at least one component attached to the conductive layer is an unpacked microcircuit chip (IC chip).

Regarding claim 15, Shindo teaches (e.g. figures 23-24, see also column 6, line 3 – column 7, line 10) an electronic module, comprising: a sheet 42, which has a first and a second surface, and which sheet includes an insulating-material layer (plastic) between the first and the second surface, a conductive pattern layer 58 on at least the

first surface of the sheet, at least one recess 44 in the sheet that extends through the second surface and the insulating-material layer as far as the conductive layer 58 on the first surface of the sheet, a component 50 having a contact surface with contact areas or contact protrusions, the component placed in the recess with the contact surface of the component facing the first surface, an electrically insulating adhesive 46 attaching the component to the conductive pattern layer on the first surface of the sheet (col. 6, ll. 31-46), and feed-throughs 54, 56 (contact holes) connecting at least some of the contact areas or contact protrusions of the component electrically to the conductive pattern layer on the first surface of the sheet.

Regarding claim 17, Shindo teaches (e.g. figures 23-24, see also col. 6, ll. 38-46) the electronic module, wherein the feed-throughs 54, 56 (contact holes) are metal (copper) and form metallurgical bonds between the contact areas or contact protrusions of the component and the conductive pattern layer.

Regarding claim 18, Shindo teaches (e.g. figures 23-24, see also column 6, line 3 – column 7, line 10) the electronic module above, wherein the component is an unpacked microcircuit chip (IC chip).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***

a. Determining the scope and contents of the prior art;
b. Ascertaining the differences between the prior art and the claims in issue;
c. Resolving the level of ordinary skill in the pertinent art; and
d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2, 6, 12-14, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shindo et al. (US 5,048,179) in view of Nakamura (US 2007/0166886).

Regarding claim 2, it is noted that Shindo do not teach the method further including at least one additional component, wherein the components are placed facing both the first and second surface in the insulating-material layer and electrical contacts are formed to the components in such a way that at least one of the components is connected to the conductive layer on the first surface and at least some one of the components is connected to the conductive layer on the second surface.

However, Nakamura teaches (e.g. figures 3-5, ¶¶ 37-44; process of forming wiring board is described in ¶¶ 45-53) the method further including at least one additional component (e.g. figure 4c), wherein the components are placed facing both the first and second surface in the insulating-material layer 12 and electrical contacts 13 are formed to the components (through 21 and 22) in such a way that at least one of the components is connected to the conductive layer on the first surface and at least some one of the components is connected to the conductive layer on the second surface (¶ 40).

Since the combination of Shindo and Nakamura teach the method above, it would have been obvious to a have the components placed facing both the first and second surface in the insulating-material layer and electrical contacts formed to the components in such a way that at least some of the components are connected to the conductive layer on the first surface and at least some to the conductive layer on the second surface of Nakamura in Shindo for the benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components.

Regarding claim 6, Nakamura teaches (e.g. figures 3-5, ¶¶ 37-44) a first and a second element are manufactured, both of which include an insulating-material layer 12, a conductive layer 13 on at least the first surface of the insulating-material layer, and at least one component 15 in at least one recess (component 15 creates a recess in layer 12), and in which method comprises: taking at least one second insulating-material sheet (12 of figure 4e), and attaching the first and the second elements 15 to each other with the aid of the said second insulating-material sheet 12, in such a way that the

second surfaces of the insulating-material layers contained in the elements (12 of figure 4d faces 12 of figure 4e) face towards each other.

Regarding claim 12, Nakamura teaches (e.g. figure 3, ¶¶ 37-44) the method above, wherein, in order to create a multi-layer circuit-board structure (e.g. figure 3), additional insulating layers 11 and conductive layers 13 are manufactured on the first and/or the second surface.

Regarding claim 13, Nakamura teaches (figures 3 and 5, ¶ 52) the components are embedded 15 in at least two sheets (12 and 13), which are subsequently attached on top of each other.

Regarding claim 14, Nakamura teaches (e.g. figure 3, ¶¶ 37-44) the method above, wherein a conductive-pattern layer 13 is manufactured on both the first and the second surfaces of the insulating-material layer 11.

Regarding claim 16, Shindo teaches (e.g. figures 23-24, see also column 6, line 3 – column 7, line 10) an electronic module, comprising:

a sheet 42, which has a first and a second surface, and which sheet includes an insulating-material layer (plastic) between the first and the second surface, a first conductive pattern layer 58 on the first surface of the sheet, at least one recess 44 in the sheet that extends through the second surface and the insulating-material layer as far as the first conductive pattern layer 58, a first component 50 having a contact surface with contact areas or contact protrusions, the first component placed in the recess with the contact surface of the first component facing the first surface, a first electrically insulating adhesive 46 attaching the first component to the first conductive

pattern layer on the first surface of the sheet (col. 6, ll. 31-46), and first feed-throughs 54, 56 (contact holes) connecting at least some of the contact areas or contact protrusions of the first component electrically to the first conductive pattern layer on the first surface of the sheet, but fails to teach a second conductive pattern layer on the second surface of the sheet, a second component placed in the insulating-material layer and facing the second conductive pattern layer, a second electrically insulating adhesive attaching the second component to the second conductive pattern layer on the second surface of the sheet, and second feed-throughs connecting at least some of the contact areas or contact protrusions of the second component electrically to the second conductive pattern layer on the second surface of the sheet.

However, Nakamura teaches (e.g. fig. 3, see also pg. 3/pps. 0037-0044) comprising: a second conductive pattern layer 13 on the second surface of the sheet 11, a second component 15 placed in the insulating-material layer and facing the second conductive pattern layer (pg. 3/pp. 0040), a second electrically insulating adhesive 12 (12 acts as an adhesive, see paragraph 7) attaching the second component 15 to the second conductive pattern layer 13 on the second surface of the sheet 11, and second feed-throughs 20 connecting at least some of the contact areas or contact protrusions of the second component 15 electrically to the second conductive pattern layer 13 on the second surface of the sheet 11.

Since the combination of Shindo and Nakamura teach the method above, it would have been obvious to a second conductive pattern layer.on the second surface of the sheet, a second component placed in the insulating-material layer and facing the

second conductive pattern layer, and electrical contacts connecting the second component to the second conductive pattern layer of Nakamura in Shindo for the benefit of providing a simple and reliable method of manufacturing electronic modules containing embedded components.

Regarding claim 19, Nakamura teaches (e.g. figure 3, ¶¶ 37-44) the electronic module above, comprising (e.g. figure 3) a further insulating layer 11 and a further conductive layer 13 on the first surface of the sheet.

8. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shindo et al. (US 5,048,179) in view of Nakamura (US 2007/0166886), and in further view of Mowatt et al. (US 5,306,670).

Regarding claim 4, Nakamura teaches said sheet 12 is a sheet which is surfaced with a conductive layer 13 on both surfaces, however the combination of Shindo and Nakamura fails to teach manufacturing at least one second recess the at least one second recess extending through the first surface and the insulating-material layer as far as the conductive layer on the second surface, which covers the manufactured recess from the direction of the second surface, taking a component, which has a contact surface with contact areas or contact protrusions, placing the component in the recess with its contact surface facing the second surface and attaching the component to the conductive layer, which covers the recess from the direction of the second surface, and forming a conductive pattern from the conductive layer covering the

recess, which pattern is electrically connected to at least some of the contact areas or contact protrusions of the component set in the recess.

However, Mowatt teaches (figures 3, 4, 6, and 7a describe the process, the sheet comprises top-most layer 12 through layer 20 of figure 4; col. 8, ll. 33-59, col. 9, ll. 27-36) manufacturing at least one second recess (through layers 124, 20, and 16 of figure 6 as shown in figure 7), the at least one second recess extending through the first surface (layer 124) and the insulating-material layer as far as the conductive layer on the second surface (18 of figure 3), which covers the manufactured recess from the direction of the second surface, taking a component (heatsink), which has a contact surface with contact areas or contact protrusions, placing the component in the recess with its contact surface facing the second surface and attaching the component to the conductive layer 18, which covers the recess from the direction of the second surface, and forming a conductive pattern (conductive layer is a conductive pattern formed in figure 3) from the conductive layer covering the recess, which pattern is electrically connected to at least some of the contact areas or contact protrusions of the component set in the recess (as shown in figure 7a).

Response to Arguments

9. With respect to the Restriction requirement, Claims 3-4 and 13 read on the elected Species I, corresponding to Figure 17. Claims 5 and 7 read on the non-elected Species III, corresponding to Figures 28 and 29.

10. With respect to Applicant's arguments filed 4/9/2008, they have been fully considered but they are not persuasive. There is lacking a discrete chronology in the process steps claimed above, the process steps only recite a correspondence between arranging components with their respective recess.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arman Khosraviani whose telephone number is (571)272-6402. The examiner can normally be reached on Monday to Friday, 7:30a - 5:00p (Eastern Time).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AK

/Steven Loke/
Supervisory Patent Examiner, Art Unit 2818